



PEBBLETECHNOLOGIES

Throw A Pebble into your Sea of Gates



Who are we

Pebble Technologies was created in 2023 by a team of engineers who shared a passion for all things digital. The team consists of a group of engineers with each member of the Pebble team bringing more than 15 years of hands-on industry experience at top-tier semiconductor companies spanning multiple areas such as communications, networking, graphics and many more.

The company is based in Athens, Greece but has members in various location over the world.



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What We do

Pebble Technologies offers a wide range of services in the fields of digital design focusing on the development of efficient solutions for a multitude of target technologies.

We can tackle any project ranging from implementing an existing specification or optimizing an existing design to seeing a project all the way from the concept phase to a prototype and then to a final verified solution both on ASIC and FPGA technologies.



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Core Expertise

FPGA

- Complete flow from system specification to verified design
- RTL development & system integration
- Rapid prototyping & PoC Development
- Accelerator development using state-of-the-art tools like HLS
- Design Verification both through functional simulation & on-chip debugging
- Extensive experience in devices from all major vendors.

ASIC

- Requirements capture & architectural exploration.
- RTL development using Verilog/SystemVerilog
- SoC Integration
- Functional Verification using UVM & OSVVM.
- Static Timing Analysis
- Physical Design for legacy and state of the art nodes.

Embedded SW

- SW development for all major embedded CPUs/MCUs
- Integration & tight-coupling between HW & SW to ensure optimal performance
- Porting & migration between different target devices & technologies.

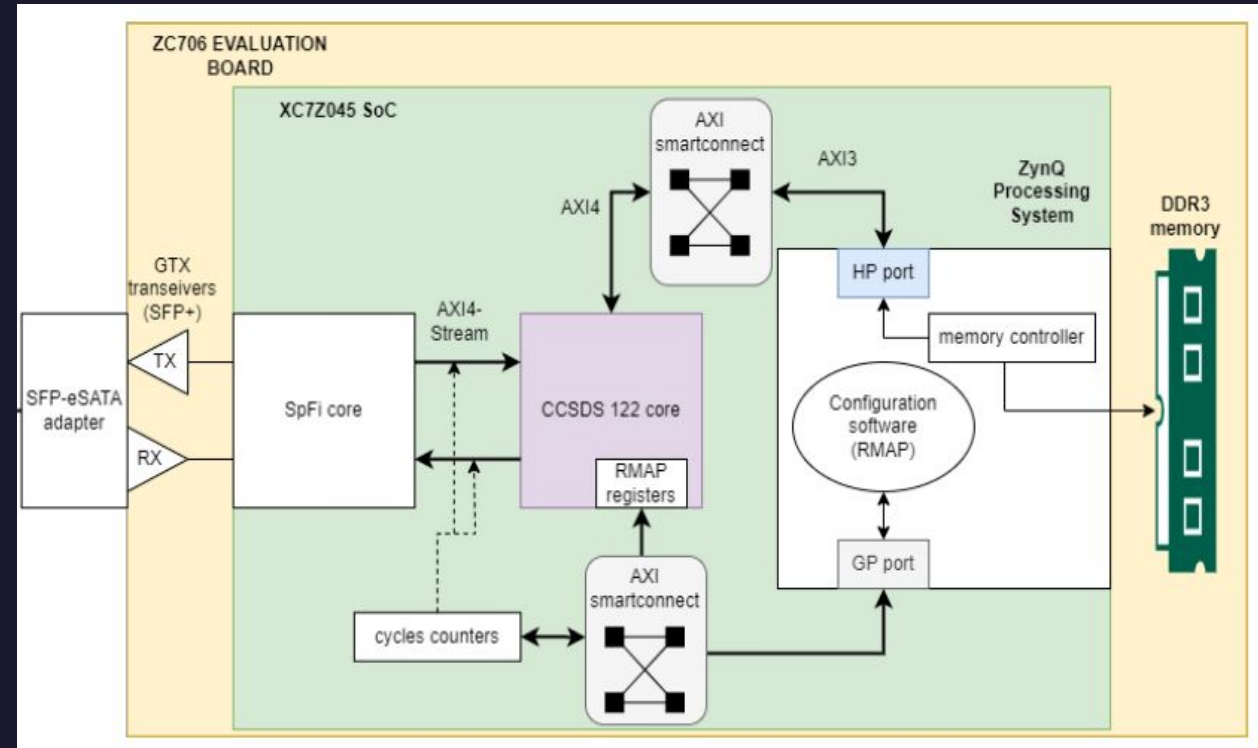
Past projects



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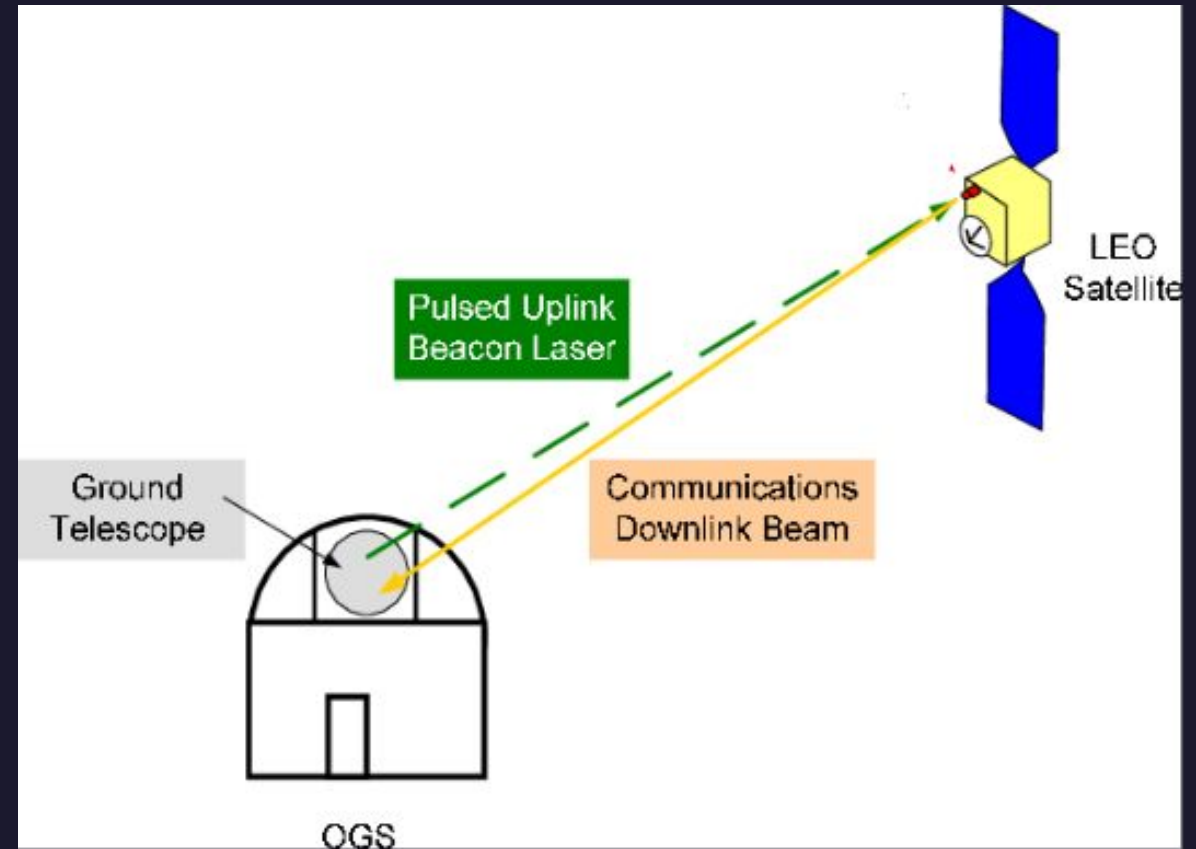
CCSDS 122.1-B-1 hyperspectral image compression

- FPGA hardware implementation of the CCSDS 122.1 standard
- Lossless and lossy compressor IP core for hyperspectral satellite images
- Design implemented on a Xilinx Zynq XC7Z045-FFG900 device
- System receives images to be processed @6.25Gbps via SpaceFibre interface, which is one of the standard high speed interfaces for space applications
- During FPGA system validation received compressed hyperspectral images, compressed images successfully compared to golden responses produced by CNES CCSDS 122.1-B-1 golden reference model



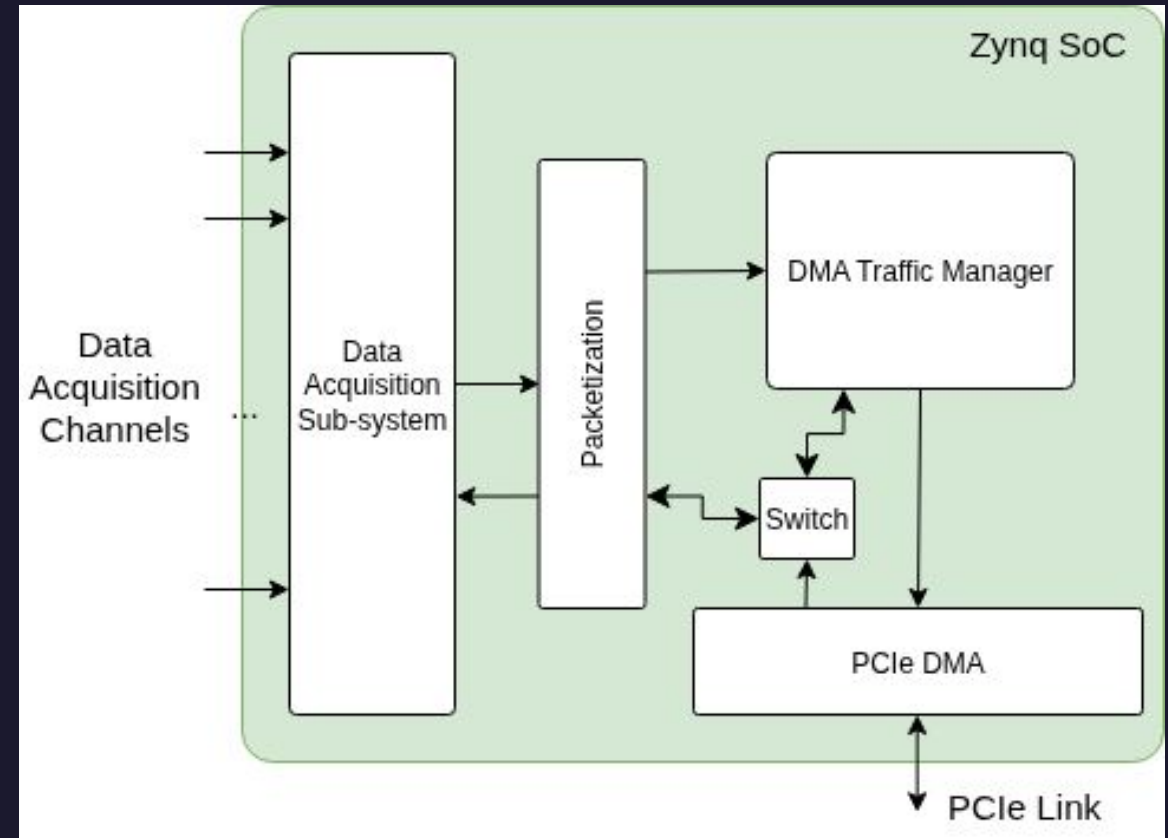
LEO satellite - laser link controller

- Design of a LEO satellite main processing and control unit on FPGA
- Control using hw/sw interface of the satellite laser communication terminal
- Laser communication is faster (up to 1 Gbps) and has better immunity against attacks compared to RF (X band) communication
- Implementation of control algorithms on FPGA (ARM Cortex-A CPU) to change the satellite orientation and process geospatial information to properly target the laser beam to the ground station
- Collect telemetries from the laser terminal and provide them to the satellite main on-board controller



High-Speed PCIe DMA Data Acquisition System

- FPGA design of a ring-buffer based PCIe DMA subsystem.
- The design ensures data acquired over sensors are efficiently transferred to a host PC.
- The system acquires data over multiple sensor, packetizes them and bundles them into PCIe DMA transactions ensuring saturation of the PCIe DMA.
- The system has been delivered to the customer and is in-production in a variety of Zynq MPSoC-based devices.



Industries

- Telecom
- Networking
- Space applications
- Image processing
- Fintech
- Manufacturing
- Consumer



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Talk to us

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